IN THE CLAIMS

Please amend the claims as indicated below:

1. **(Currently Amended)** A system for providing parallel processing of data to a plurality of digital signal processors (DSPs), comprising:

means for transmitting communication data to a load management system from ~~a CPU;~~ at least one CPU, wherein the load management system includes:

a plurality of direct memory access (DMA) devices, each DMA device having one or more internal registers, one or more FIFOs, and a state machine associated with the one or more FIFOs;

a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and control registers coupled to the plurality of DMA devices;

at least one CPU interface for interfacing the at least one CPU with the plurality of status and control registers; and

a plurality of DSP interfaces for interfacing the plurality of DSPs with the plurality of DMA devices;

means for selecting ~~a digital signal processor (DSP) from a plurality~~ two or more DSPs from the plurality of DSPs for processing the communication data;

means for processing the communication data using the selected ~~DSP~~ two or more DSPs; and

means for transmitting the processed communication data back to ~~the CPU~~ the at least one CPU and to a communication device.

2. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication data is transmitted from a VoIP ~~medium~~ system.

3. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication data is transmitted from a FoP ~~medium~~ system.

4. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication

data is transmitted from an IP to sonet ~~medium~~ system.

5. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication data is transmitted from an encoder/decoder.

6. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication data is transmitted from a broadband communication ~~medium~~ system.

7. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication data is transmitted from an image processing ~~medium~~ system.

8. **(Currently Amended)** ~~A system~~ The system of claim 1, wherein the communication data is transmitted from a data modem.

9. **(Canceled).**

10. **(Currently Amended)** ~~A system of claim 9~~ The system of claim 1, wherein ~~the DSP interface~~ each of the plurality of DSP interfaces includes a program/data memory and a ping pong memory.

11. **(Currently Amended)** ~~A system of claim 9~~ The system of claim 1 further comprising an external memory, wherein the external memory is coupled to the plurality of DSPs through a plurality of dedicated memory threads.

12. **(Currently Amended)** ~~A system of claim 9~~ The system of claim 1, wherein ~~the CPU~~ the at least one CPU interface includes ~~a routing~~ at least one routing MUX, wherein ~~the routing~~ the at least one routing MUX is coupled to the external memory device.

13. **(Currently Amended)** ~~A system~~ The system of claim 12, wherein the external memory device comprises a memory access controller array.

14. **(Currently Amended)** ~~A system~~ The system of claim 12, wherein the external memory device comprises a memory management system.

15-32. (Canceled).

33. (New) A method for providing parallel processing of data to a plurality of digital signal processors (DSPs), comprising the steps of:

transmitting communication data to a load management system from at least one CPU,

wherein the load management system includes:

a plurality of direct memory access (DMA) devices, each DMA device having one or more internal registers, one or more FIFOs, and a state machine associated with the one or more FIFOs;

a memory interface for interfacing the plurality of DMA devices with an external memory device;

a plurality of status and control registers coupled to the plurality of DMA devices;

at least one CPU interface for interfacing the at least one CPU with the plurality of status and control registers; and

a plurality of DSP interfaces for interfacing the plurality of DSPs with the plurality of DMA devices;

selecting two or more DSPs from the plurality of DSPs for processing the communication data;

processing the communication data using the selected two or more DSPs; and

transmitting the processed communication data back to the at least one CPU and to a communication device.